

## High-Speed Up/Down Counter Board for PCI Express CNT-3208M-PE



\* Specifications, color and design of the products are subject to change without notice.

### Features

**8ch 32-bit up/down counter, high speed pulse input of 10MHz, and disconnection detection are available.**

A 32-bit up/down counter with 8 channels is mounted on one board, high speed pulse input up to 10MHz (unisolated TTL-level input, differential line receiver) is available, and disconnection detection can be performed for differential line receiver input.

2-phase signals and 1-phase signals such as a rotary encoder or linear scale can be counted. Surge protection is realized by implementing protectors in the input circuit.

In addition, 1pin/ch of control input signal is provided. It can be used as counter start/stop, preset, zero clear, general-purpose input.

**Bus master transfer function is provided.**

Bus master transfer makes it possible to transfer large data at a high speed without extra CPU load at a sampling rate up to 20MHz.

**Digital filter function to prevent wrong recognition of input signals due to noises is provided.**

Digital filter function by which noises of counter input signals (phase-A, phase-B, phase-Z) and control input signals can be prevented is equipped. Digital filter can either be not used or set within the range of 0.1μ - 1.6384msec by software.

In addition, as all these input signals are taken into the internal counter via the digital filter, when using the digital filter, these signals are taken in with a delay of a specified duration.

**Windows compatible driver librarie is attached.**

Using the attached driver library API-PAC(W32) makes it possible to create applications of Windows. In addition, a diagnostic program by which the operations of hardware (interrupt, I/O address, I/O status) can be checked is provided.

**The synchronization control connectors are provided**

The synchronization control connectors which can make boards up to 16 pieces synchronously run are provided. In addition, the synchronous operation with CONTEC boards where a synchronization control connector is mounted can be easily realized.

**The input circuit has a built-in varistor for voltage surge protection**

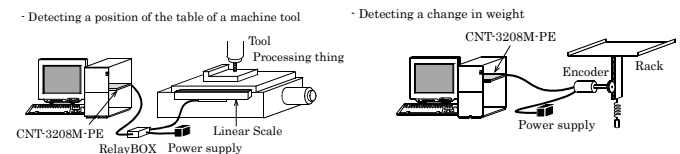
To protect the input circuit from voltage surges, a varistor is connected.

This product is a PCI Express bus compliant counter input board which counts the pulse signal input from an external device.

8 ch 32-bit up/down counter is mounted, and the bus master transfer function makes it possible to transfer data at a high speed by high speed pulse input (unisolated TTL-level input, differential line receiver) up to 10MHz. In addition, 2-phase signals and 1-phase signals such as a rotary encoder or linear scale can be counted.

With the driver libraries for Windows supplied as standard, applications with CONTEC hardware features fully utilized can be created.

< Example >



\*The contents in this document are subject to change without notice.

\*Visit the CONTEC website to check the latest details in the document.

\*The information in the data sheets is as of June, 2022.

**Functions and connectors are compatible with PCI compatible board CNT32-8M(PCI).**

The functions same with PCI compatible board CNT32-8M(PCI) are provided. In addition, as there is compatibility in terms of connector shape and pin assignments, it is easy to migrate from the existing system.

**Independent general-purpose timer is provided**

The timer which can let interrupts occur at a specified interval is provided.

The timer can be set within the range of 1 - 6553msec (selectable in step of 1 msec).

## Specifications

### Specifications < 1 / 2 >

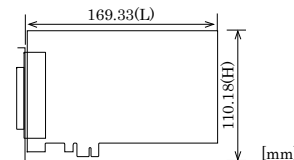
Item	Specifications
<b>Input</b>	
<b>Counter</b>	
Channel count	8 ch
Count system	Up / down counting (2-phase / Single-phase / Single-phase Input with Gate Control Attached)
Max. count	FFFFFFFF (binary data, 32Bit)
Input type	Differential line receiver input or Unisolated TTL level input (Selectable by software)
Input signal	Phase-A/UP One x 8 ch Phase-B/DOWN One x 8 ch Phase-Z/CLR One x 8 ch
Differential line receiver input section	Element in use : Equivalent to AM26LS32 (T.I.) Terminating resistance : 150Ω (Can be disconnected switch.) Receiver input sensitivity : ±200mV In-phase input voltage range : 0 - +7V Signal extension distance : 1200m (dependent on wiring environment and input frequency) *1, *2
TTL level input section*3	Element in use : Equivalent to 74ALS41NS (T.I.) Signal extension distance : 1.5m (dependent on wiring environment)
Response frequency (Max.)	10MHz 50% duty
Digital filter	0.1μsec - 1.6384msec or not used (can be independently set for each channel)
Timer	1msec - 6553msec 1msec unit
Counter start trigger	Software / External start input / Sampling start trigger
Counter stop trigger	Software / External start input / Sampling stop trigger
<b>Input</b>	
<b>Sampling*3</b>	
Sampling start trigger	Software / External start input / Sync control connectors / Count match
Sampling stop trigger	Software / External stop input / Specification number / Bus master transfer error / Sync control connectors / Count match
Sampling clock	Sampling timer / External clock input / Sync control connectors
Sampling timer	50nsec - 107sec 25nsec unit (can not be independently set for each channel)
External sampling start signal	TTL level (Select Rise or Fall)
External sampling stop signal	TTL level (Select Rise or Fall)
External sampling clock signal	TTL level (Fall)
Response frequency (Max.)	10MHz 50% duty
<b>Control*3</b>	
Control input signal type	Unisolated TTL level
Control input channel	One x 8 ch
Control input signal	- Preset (Select Rise or Fall) - Zero-clear (Select Rise or Fall) - Counter start / stop (Select Rise or Fall) - General-purpose input (positive logic) Software-selected from among the above four options
Response time (Max.)	100nsec
Interrupt factor	Count match (16 ch), Counter error (2 ch), Sampling factor (6 ch), Sync control connectors error (2 ch), Carry / Borrow (1 ch), Timer (1 ch)
<b>Output*3</b>	
<b>Control</b>	
Control output channel	One x 8 ch
Control output signal	- Count match 0 output (one-shot pulse output) - Count match 1 output (one-shot pulse output) - Digital filter error output (one-shot pulse output) - Abnormal input error output (one-shot pulse output) - Disconnection alarm error output (one-shot pulse output) - General-purpose output (Level output) Software-selected from among the above five options (Positive / negative logic is selected with the on-board switch.)
One shot output signal amplitude	Selected between 10μsec, 100μsec, 1msec, 10msec and 100msec (Can be set for each channel, within precision + 1μsec)
Element in use	Non-Isolated Open Collector Output : Equivalent to 74LS07NS (T.I.)
Output rating	30VDC 40mA
Response speed (Max.)	5μsec
<b>TP</b>	
Test pulse output signal	One line receiver output for each of phases-A and B (For TTL level output, use the positive line receiver output.)
Element in use	Equivalent to AM26LS31 (T.I.)
Frequency	100kHz

### Specifications < 2 / 2 >

Item	Specifications
<b>Bus master</b>	
DMA channel	1 ch
Transfer bus width	32-Bit width
Transfer data length	8 PCI Words length (Max.)
Transfer rate	80MB / sec (Max.133MB / sec)
FIFO	1K-DWord
Scatter/Gather function	64MB
Interrupt factor	Bus master event (7 ch)
<b>Synchronization</b>	
Control output signal	Select the output signal by software when setting the synchronization master board.
Control input signal	Select the synchronization factor by software when setting the synchronization slave mode.
Connectable number of device	16 boards including the master board
<b>Common</b>	
I/O address	Occupies 2 locations, any 32-bytets and 64-byte boundary
Additional function	Filter function, count match pulse output, test pulse output, disconnection alarm detection
Power consumption (Max.)	3.3VDC 1.8A
Operating condition	0 - 50°C, 10 - 90%RH (No condensation)
Bus specification	PCI Express Base Specification Rev. 1.0a x1
Dimension (mm)	169.33(L) x 110.18(H)
Connector used	CN1 : 96-pin half-pitch connector PCR-E96LMD [mfd by HONDA TSUSHIN KOGYO CO., LTD.] or equivalent to it CN2, CN3 : PS-10PE-D4T1-B1 [JAE] or equivalent to it x 2
Weight	160g
Standard	VCCI Class A, CE Marking (EMC Directive Class A, RoHS Directive), UKCA

- \*1 The frequency response at an extension of 50 m is about 10 MHz (depending on the wiring environment).  
The frequency response at an extension of 100 m is about 5 MHz (depending on the wiring environment).  
The frequency response at an extension of 150 m is about 1.5 MHz (depending on the wiring environment).  
The frequency response at an extension of 300 m is about 1 MHz (depending on the wiring environment).  
The frequency response at an extension of 600 m is about 500 KHz (depending on the wiring environment).  
The frequency response at an extension of 1200 m is about 80 KHz (depending on the wiring environment).
- \*2 Please use the shielded cable with a length of less than 30m to meet "CE EMC Directive".
- \*3 Please use the shielded cable to meet "CE EMC Directive".

### Board Dimensions



The standard outside dimension (L) is the distance from the end of the board to the outer surface of the slot cover.

### Difference in bus mastering transfer rate by system configuration

	Limited	Unlimited
430TX/Pentium233MHz	20	13.4
440BX/PentiumII450MHz	20	13.4
i820/PentiumIII800MHz	20	13.4
i815E/PentiumIII800MHz	20	13.4

[MHz]

"Limited" indicates that the number of transfers is specified; "Unlimited" specifies that it is not specified.

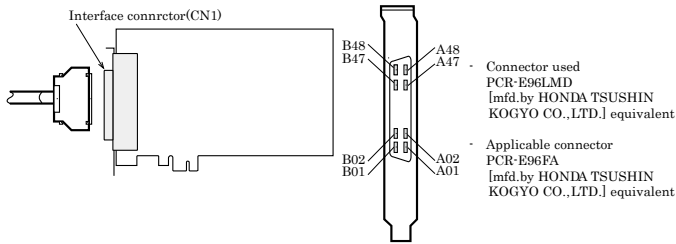
These values may not be satisfied depending on the system configuration including other boards and applications.



## How to connect the connectors

### Connector shape

The on-board interface connector (CN1) is used when connecting this product and the external devices.



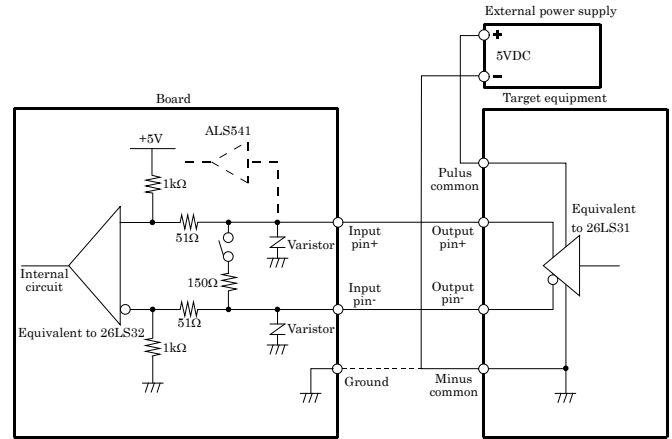
### Connector Pin Assignment

Ground	GND	[149]	[1]	Ground	Ground
CH7 differential Phase-Z input	D7Z	[148]	[2]	CH3 differential Phase-Z input	CH3 differential Phase-Z input
CH7 TTL Phase-Z input/Differential Phase-Z input	T7Z/D7Z	[147]	[3]	CH3 differential Phase-Z input/TTL Phase-Z input	CH3 differential Phase-Z input/TTL Phase-Z input
CH7 differential Phase-B input	D7B	[146]	[4]	CH3 differential Phase-B input	CH3 differential Phase-B input
CH7 TTL Phase-B input/Differential Phase-B input	T7B/D7B	[145]	[5]	CH3 differential Phase-B input/TTL Phase-B input	CH3 differential Phase-B input/TTL Phase-B input
CH7 differential Phase-A input	D7A	[144]	[6]	CH3 differential Phase-A input	CH3 differential Phase-A input
CH7 TTL Phase-A input/Differential Phase-A input	T7A/D7A	[143]	[7]	CH3 differential Phase-A input/TTL Phase-A input	CH3 differential Phase-A input/TTL Phase-A input
Ground	GND	[142]	[8]	Ground	Ground
CH6 differential Phase-Z input	D6Z	[141]	[9]	CH2 differential Phase-Z input	CH2 differential Phase-Z input
CH6 TTL Phase-Z input/Differential Phase-Z input	T6Z/D6Z	[140]	[10]	CH2 differential Phase-Z input/TTL Phase-Z input	CH2 differential Phase-Z input/TTL Phase-Z input
CH6 differential Phase-B input	D6B	[139]	[11]	CH2 differential Phase-B input	CH2 differential Phase-B input
CH6 TTL Phase-B input/Differential Phase-B input	T6B/D6B	[138]	[12]	CH2 differential Phase-B input/TTL Phase-B input	CH2 differential Phase-B input/TTL Phase-B input
CH6 differential Phase-A input	D6A	[137]	[13]	CH2 differential Phase-A input	CH2 differential Phase-A input
CH6 TTL Phase-A input/Differential Phase-A input	T6A/D6A	[136]	[14]	CH2 differential Phase-A input/TTL Phase-A input	CH2 differential Phase-A input/TTL Phase-A input
Ground	GND	[135]	[15]	Ground	Ground
CH5 differential Phase-Z input	D5Z	[134]	[16]	CH1 differential Phase-Z input	CH1 differential Phase-Z input
CH5 TTL Phase-Z input/Differential Phase-Z input	T5Z/D5Z	[133]	[17]	CH1 differential Phase-Z input/TTL Phase-Z input	CH1 differential Phase-Z input/TTL Phase-Z input
CH5 differential Phase-B input	D5B	[132]	[18]	CH1 differential Phase-B input	CH1 differential Phase-B input
CH5 TTL Phase-B input/Differential Phase-B input	T5B/D5B	[131]	[19]	CH1 differential Phase-B input/TTL Phase-B input	CH1 differential Phase-B input/TTL Phase-B input
CH5 differential Phase-A input	D5A	[130]	[20]	CH1 differential Phase-A input	CH1 differential Phase-A input
CH5 TTL Phase-A input/Differential Phase-A input	T5A/D5A	[129]	[21]	CH1 differential Phase-A input/TTL Phase-A input	CH1 differential Phase-A input/TTL Phase-A input
Ground	GND	[128]	[22]	Ground	Ground
CH4 differential Phase-Z input	D4Z	[127]	[23]	CH0 differential Phase-Z input	CH0 differential Phase-Z input
CH4 TTL Phase-Z input/Differential Phase-Z input	T4Z/D4Z	[126]	[24]	CH0 differential Phase-Z input/TTL Phase-Z input	CH0 differential Phase-Z input/TTL Phase-Z input
CH4 differential Phase-B input	D4B	[125]	[25]	CH0 differential Phase-B input	CH0 differential Phase-B input
CH4 TTL Phase-B input/Differential Phase-B input	T4B/D4B	[124]	[26]	CH0 differential Phase-B input/TTL Phase-B input	CH0 differential Phase-B input/TTL Phase-B input
CH4 differential Phase-A input	D4A	[123]	[27]	CH0 differential Phase-A input	CH0 differential Phase-A input
CH4 TTL Phase-A input/Differential Phase-A input	T4A/D4A	[122]	[28]	CH0 differential Phase-A input/TTL Phase-A input	CH0 differential Phase-A input/TTL Phase-A input
Ground	GND	[121]	[29]	Ground	Ground
CH7 control input *1	D17	[120]	[30]	CH3 control input *1	CH3 control input *1
CH6 control input *1	D16	[119]	[31]	CH2 control input *1	CH2 control input *1
CH5 control input *1	D15	[118]	[32]	CH1 control input *1	CH1 control input *1
CH4 control input *1	D14	[117]	[33]	CH0 control input *1	CH0 control input *1
External sampling start signal input	EXTSTART	[116]	[34]	External sampling clock input	External sampling clock input
External sampling stop signal input	EXTSTOP	[115]	[35]	Ground	Ground
CH7 control output *2	D07	[114]	[36]	CH3 control output *2	CH3 control output *2
CH6 control output *2	D06	[113]	[37]	CH2 control output *2	CH2 control output *2
CH5 control output *2	D05	[112]	[38]	CH1 control output *2	CH1 control output *2
CH4 control output *2	D04	[111]	[39]	CH0 control output *2	CH0 control output *2
Ground	GND	[110]	[40]	Ground	Ground
Test pulse differential Phase-B output	TP0B	[109]	[41]	Test pulse differential Phase-B output	Test pulse differential Phase-B output
Test pulse TTL Phase-A output/Differential Phase-A output	TP0A	[108]	[42]	Test pulse differential Phase-A output/TTL Phase-A output	Test pulse differential Phase-A output/TTL Phase-A output

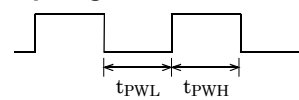
\* The numbers in square brackets [ ] are pin numbers designated by HONDA TSUSHIN KOGYO CO., LTD.

\*1 The control inputs can serve as the general-purpose, counter start/stop, preset, and zero-clear inputs.

\*2 The control outputs can serve as the general-purpose output, count match, abnormal input error, digital filter error, and discontinuity alarm error outputs.



### Input signal



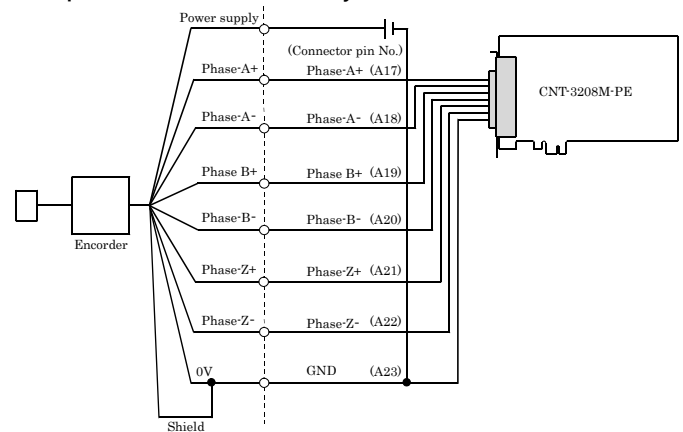
tpWH : High-level count input pulse width 50nsec (Min.)

tpWL : Low-level count input pulse width 50nsec (Min.)

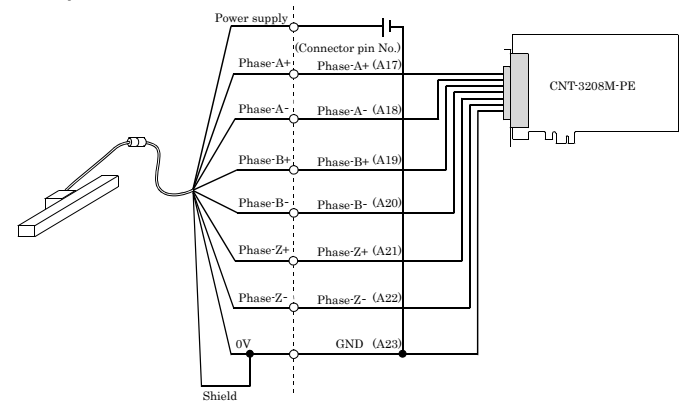
### CAUTION

- In the input pin+, TTL level input circuit is parallel-connected.
- Please use the shielded cable with a length of less than 30m to meet "CE EMC Directive".

### Example Connection with a Rotary Encoder



### Example Connection with a Linear Scale



## External Device Connection 1 -differential line receiver input-

### Connecting the differential line receiver input

Use the differential line receiver input to connect the board to the line receiver output circuit of a rotary encoder or linear scale. The maximum input frequency is 10 MHz.

For use in two-phase input mode, connect both of the phase-A and phase-B inputs. For use in single-phase input mode, connect either of them. If phase-Z is not used, the input need not be connected.

For differential line receiver input mode, you can select whether to insert the terminal resistor.

### Detailed description of differential line receiver input circuit

To protect the input circuit from voltage surges, a varistor is connected.

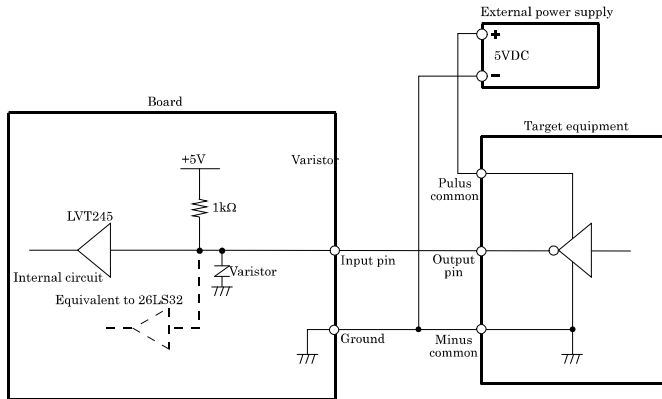
## External Device Connection 2 -TTL level input-

### Connecting the TTL level input

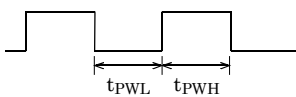
Use the TTL-compatible input to connect the board to the TTL-compatible output circuit of a rotary encoder or linear scale. The maximum input frequency is 10 MHz.

For use in two-phase input mode, connect both of the phase-A and phase-B inputs. For use in single-phase input mode, connect either of them. If phase-Z is not used, the input need not be connected.

### Detailed description of TTL level input circuit



### Input signal



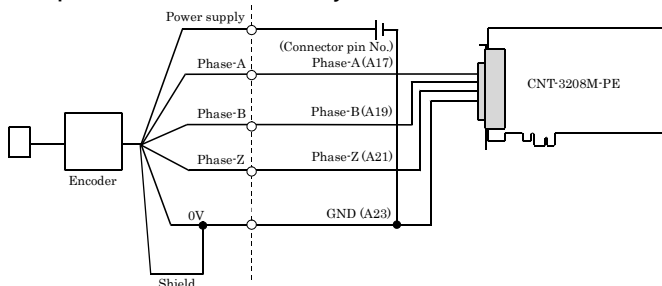
$t_{pWH}$  : High-level count input pulse width 50nsec (Min.)

$t_{pWL}$  : Low-level count input pulse width 50nsec (Min.)

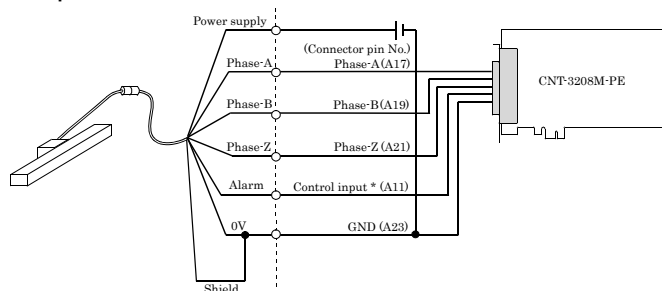
### CAUTION

- The connection cable length should be within 1.5 m.
- To prevent noise from causing a malfunction, arrange the connection cable as away from any other signal conductor or noise source as possible.
- In the input pin+, TTL level input circuit is parallel-connected.
- Please use the shielded cable to meet "CE EMC Directive".

### Example Connection with a Rotary Encoder



### Example Connection with a Linear Scale



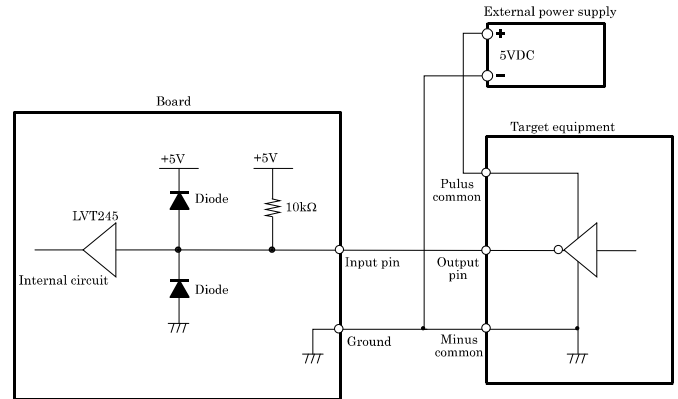
\* When the control input is set as a general-purpose input, the alarm output state can be checked. When the control input is set as the counter stop input, the counter can be stopped at alarm output.

## Connecting the control signal input/output

### Connection of a control input

For control signal input, the board has one pin per channel to be used to selectively start/stop or preset the counter for the channel and one pin per channel to be used to start or stop the sampling clock.

### Control input circuit and its sample connection



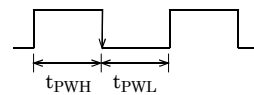
### CAUTION

- The connection cable length should be within 1.5 m.
- To prevent noise from causing a malfunction, arrange the connection cable as away from any other signal conductor or noise source as possible.
- Please use the shielded cable to meet "CE EMC Directive".

### External sampling clock signal (EXTCLK)

This pin feeds the external pacer clock signal. The maximum frequency is 10 MHz. When the sampling clock input has been set to the external clock input, sampling is performed at the falling edge of the signal at this pin.

### EXTCLK

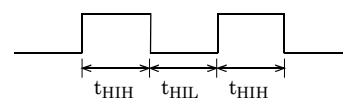


$t_{pWH}$  : High-level clock pulse width 50nsec (Min.)

$t_{pWL}$  : Low-level clock pulse width 50nsec (Min.)

### Other control input signals (DI0 - DI7, EXTSTART, EXTSTOP)

Control input signal can be selected with whether to enable rise or fall by software at the TTL level. High- and low-level hold times of at least 50 nsec are required to detect an edge of the signal.



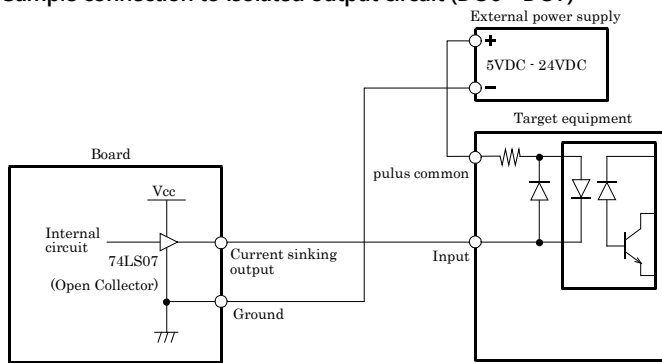
$t_{HIH}$  : High-level hold time 50nsec (Min.)

$t_{HIL}$  : Low-level hold time 50nsec (Min.)

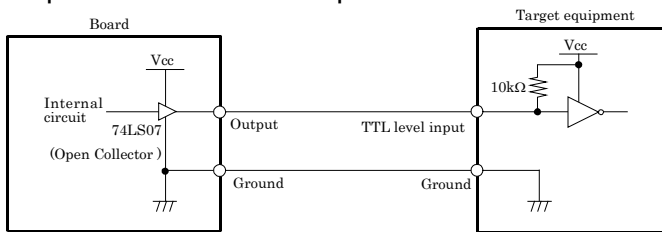
### Connection of a control output

The control output of the board provides the general-purpose output signal (level output) and the one-shot pulse signals that indicate hardware events such as a count match. For the signal output, positive or negative logic can be selected with SW2.

### Sample connection to Isolated output circuit (DO0 - DO7)



### Sample connection to TTL level input circuit



#### ⚠ CAUTION

- The output of this board has no surge voltage protector. To drive an inductive load such as a relay or lamp using this board, apply surge voltage protection to the load side. For surge voltage protection, see "Surge Voltage Countermeasures" in the next section.
- Please use the shielded cable to meet "CE EMC Directive".